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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,511	07/13/2001	Gyudong Kim	19570-06205	3384

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EXAMINER	
WILLIAMS, LAWRENCE B	

ART UNIT	PAPER NUMBER
2634	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,511	KIM ET AL.	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-38; 44-50* is/are allowed.

6)☒ Claim(s) *1-12,16,17,19-22,26,27,29 and 30* is/are rejected.

7)☒ Claim(s) *13-15,18,23-25,28,31-33 and 40-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3-5, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelkar et al. (US Patent 5,828,255).

(1) With regard to claim 1, Kelkar et al. discloses in Figs. 4-6, a method of reducing jitter in data transmission between a transmitter and a receiver, where the receiver has a phase-locked loop (PLL) (701) with a loop bandwidth for recovering the clock and data from the transmitter, the method comprising the steps of: measuring relative jitter (703) between the recovered clock and the recovered data at the receiver and adaptively adjusting the PLL loop bandwidth of the receiver to reduce the relative jitter (abstract; col. 9, line 60 - col. 10, line 14).

(2) With regard to claim 3, claim 3 inherits all limitations of claim 1. Furthermore, though Kelkar et al does not explicitly disclose the PLL for generating both the clock and the

data, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating both the clock and data.

(3) With regard to claim 4, claim 4 inherits all limitations of claim 1. Furthermore, though Kelkar et al. does not explicitly disclose the PLL for generating both the clock and the data, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating both the data.

(4) With regard to claim 5, Kelkar et al. discloses in Figs. 4-6, a system for reducing jitter in data transmission between a transmitter and a receiver, where the receiver has a phase-locked loop (PLL) (701) with a loop bandwidth for recovering the clock and data from the transmitter, the system comprising: means for measuring relative jitter (701) between the recovered clock and the recovered data at the receiver; and means for adaptively adjusting the PLL loop bandwidth (715, 717) of the receiver to reduce the relative jitter.

(5) With regard to claim 7, claim 7 inherits all limitations of claim 5. Furthermore, though Kelkar et al does not explicitly disclose the PLL for generating both the clock and the data, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating both the clock and data.

(6) With regard to claim 8, claim 8 inherits all limitations of claim 5. Furthermore, though Kelkar et al. does not explicitly disclose the PLL for generating both the clock and the data, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating both the data.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent 5,828,255) as applied to claims 1 and 5 above, and further in view of Ahn et al. (US 2002/0064247 A1).

(1) With regard to claim 2, claim 2 inherits all limitations of claim 1 above. As noted above, Kelkar et al. discloses all limitations of claim 1 above. Kelkar et al. does not however disclose wherein said relative jitter is represented by the activity of a phase pointer indicating a correct data sampling point. However, Ahn et al. discloses wherein said relative jitter is represented by the activity of a phase pointer indicating a correct data sampling point [0058].

One skilled in the art would have clearly recognized that wherein said relative jitter is epresented by the activity of a phase pointer indicating a correct data sampling point is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Ahn et al. to modify the invention of Kelkar et al. as a method of reducing substantial distortion in a received signal [0007].

(2) With regard to claim 6, claim 6 inherits all limitations of claims 2 and 5 above.

6. Claims 9, 10-12, 16-17, 19-22, 26-27, 29-30, 33, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent 5,828,255) in view of Ahn et al. (US 2002/0064247 A1).

(1) With regard to claim 9, Kelkar et al. discloses in Figs. 4-6, a method of reducing jitter in data transmission between a transmitter and a receiver, where the receiver has a phase-locked loop (PLL) (701) with a loop bandwidth for recovering the clock and data from the transmitter, the method comprising the steps of: adaptively adjusting a characteristic of the receiver reduce the relative jitter (abstract; col. 9, line 60 - col. 10, line 14). Kelkar et al does not however teach the method comprising the steps of: measuring phase pointer activity where the phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver; and adaptively adjusting a characteristic of the receiver so as to reduce the phase pointer activity.

However, Ahn et al. discloses measuring phase pointer activity where the phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver [0058].

One skilled in the art would have clearly recognized that measuring phase pointer activity where the phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Ahn et al. to modify the invention of Kelkar et al. as a method of reducing substantial distortion in a received signal [0007].

(2) With regard to claim 10, Kelkar et al. also discloses wherein said characteristic of the receiver includes the receiver PLL loop bandwidth (col. 9, line 60 - col. 10, line 14).

(3) With regard to claim 11, Ahn et al. also discloses in Fig. 1, wherein said phase pointer is selected from oversampled points.

(4) With regard to claim 12, Ahn et al. also discloses wherein said phase pointer is determined from a digital tracking pointer representing the phase changes of the received data [0058-0059].

(5) With regard to claim 16, claim 16 inherits all limitations of claims 1 and 3, above.

(6) With regard to claim 17, claim 17 inherits all limitations of claims 1 and 4, above.

(7) With regard to claim 19, claim 19 inherits all limitations of claim 9 as claim 19 only discloses a system for implementing the method of claim 9.

(8) With regard to claim 20, claim 20 inherits all limitations of claims 19 and 10, above.

(9) With regard to claim 21, claim 21 inherits all limitations of claims 19 and 11, above.

(10) With regard to claim 22, claim 22 inherits all limitations of claims 19 and 12, above.

(11) With regard to claim 26, claim 26 inherits all limitations of claims 19 and 16, above.

(12) With regard to claim 27, claim 27 inherits all limitations of claims 19 and 17, above.

(13) With regard to claim 29, claim 29 inherits all the limitations of claims of 19 and 20 and claim 29 only discloses the method of the system disclosed in claims 19 and 20.

(14) With regard to claim 30, claim 30 inherits all limitations of claims 29 and 21 above.

(15) With regard to claim 33, though both inventers are silent as to the encoding schemes involved in the data, it would be inherent to one skilled in the art that the type encoding would be irrelevant, since both inventions are geared toward the measurement of jitter and removal therof.

(16) With regard to claim 39, claim 39, inherits all limitations of claim 19, above.

Allowable Subject Matter

7. Claims 34-38; 44-50 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a scheme for reducing jitter in a data communication syste. Prior art fails to teach a scheme comprising; "a phase-tracking unit for tracking a phase pointer representing a relative jitter between the recovered data and clock; control logic for measuring the activity of the phase pointer to produce a control signal; and loop bandwidth of the PLL can be adjusted based on the control signal from the control logic" or "measuring the phase pointer activity in DC and AC components; and adjusting the phase pointer activity by compensating for the DC component of the phase pointer activity" as disclosed in claims 34 and 44, respectively.

9. Claims 13-15, 18, 23-25, 28, 31-33, 40-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Amick et al discloses in US Patent 6,614,275 B1 Adjustable Capacitances for DLL Loop and Power Supply Noise Filters.

b.) Kerner discloses in US Patent 6,307,411 B1 Wide Tracking Range, Auto Ranging, Low Jitter Phase Lock for Swept and Fixed Frequency Systems.

c.) Hoffman et al. discloses in US Patent 6,151,076 a System For Phase-Locking a Clock to a Digital Audio signal Embedded in a Digital Video Signal.

d.) Ke et al. discloses in US Patent 6,696,886 B1 an Automatically Adjusting Gain/Bandwidth Loop Filter.

e.) Sun discloses in US Patent 5,056,118 a Method and Apparatus for Clock and Data Recovery with High Jitter Tolerance.

f.) Wei discloses in US 2004/0001567 A1 dynamic Phase Tracking Using Edge Detection.

g.) Blazo et al. discloses in US Patent 5,757,652 electrical Signal Jitter and Wander Measurement System and Method.

h.) Butcher discloses in US Patent 4,789,996 Center Frequency High Resolution Digital Phase-Lock Loop Circuit.

i.) Ellersick et al. discloses in US Patent 6,044,122 Digital Phase Acquisition With Delay Locked Loop.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
November 2, 2004

Amanda Le

AMANDA T. LE
PRIMARY EXAMINER